



FORM PTO-1449

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICEATTY. DOCKET NO.
174/205APPLICATION NO.
09/826,527INFORMATION DISCLOSURE
STATEMENT BY APPLICANTAPPLICANT
Martin LanghammerFILING DATE
April 4, 2001GROUP
2121

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
						<i>RECEIVED</i>
						<i>JUL 27 2001</i>
						<i>Technology Center 2100</i>

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION
<i>Mar</i>	A. Chhabra and R. Iyer, "A Block Floating Point Implementation on the TMS320C54x DSP", Application Report SPRA610, Texas Instruments, December 1999, pp. 1-10.					
<i>Mar</i>	The Applications Engineering Staff of Analog Devices, DSP Division, <u>Digital Signal Processing Applications Using the ADSP-2100 Family</u> (edited by Amy Mar), Prentice-Hall, Inc., Englewood Cliffs, NJ, Copyright 1990 by Analog Devices, Inc., Norwood, MA, pp. 141-192.					
<i>Mar</i>	"TMS320C54x DSP Reference Set, Volume 1: CPU and Peripherals", Literature Number: SPRU131F, Texas Instruments, April 1999, pp. 2-1 through 2-16 and 4-1 through 4-29.					

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EXAMINER INITIAL	
	A. Chhabra and R. Iyer, "A Block Floating Point Implementation on the TMS320C54x DSP", Application Report SPRA610, Texas Instruments, December 1999, pp. 1-10.
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Sheet 1 of 2

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U.S. PATENTS

EXAMINER INITIAL	PATENT NUMBER	DATE (MM/DD/YY)	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
man	3,473,160	10/14/69	Wahlstrom	340	172.5	
	4,871,930	10/03/89	Wong et al.	307	465	
	4,912,345	03/27/90	Steele et al.	307	465	
	5,122,685	06/16/92	Chan et al.	307	465.1	
	5,128,559	07/07/92	Steele	307	465	
	5,371,422	12/06/94	Patel et al.	326	41	
	5,483,178	01/09/96	Costello et al.	326	41	
	5,689,195	11/18/97	Cliff et al.	326	41	
	5,754,459	05/19/98	Telikepalli	364	759	
	5,825,202	10/20/98	Tavana et al.	326	39	
	5,874,834	02/23/99	New	326	39	
	6,069,487	05/30/00	Lane et al.	326	37	
	6,215,326 B1	04/10/01	Jefferson et al.	326	41	04/10/01

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U.S. PATENT APPLICATIONS

EXAMINER INITIAL	APPLICATION NUMBER	FILING DATE (MM/DD/YY)	NAME
man	09/124,649	07/29/98	Ngai et al.
	09/389,995	09/02/99	Heile
	09/516,921	03/02/00	Ngai et al.
	09/924,354	08/07/01	Langhammer et al.
	09/955,645	09/18/01	Langhammer et al.
	09/969,977	10/02/01	Langhammer

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE (MM/DD/YY)	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
man	0 461 798 A2	12/18/91	EPO	H03K	19/177		
man	2 283 602 A	05/10/95	GB	H03K	19/177		

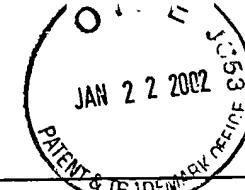
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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER INITIAL	[REDACTED]
<i>Mar</i>	"Implementing Multipliers in FLEX 10K EABs", Technical Brief 5, Altera Corporation, March 1996.
	"Xilinx Unveils New FPGA Architecture to Enable High-Performance, 10 Million System Gate Designs", Xilinx Virtex-II Architecture Technology Backgrounder, Xilinx Inc., June 22, 2000, pp.1-9.
	"Xilinx Announces DSP Algorithms, Tools and Features for Virtex-II Architecture", Xilinx Inc., November 21, 2000, pp. 1-4.
	"Virtex-II 1.5V Field-Programmable Gate Arrays", Advance Product Specification, DS031-2 (v1.3), Xilinx Inc., January 25, 2001, Module 2 of 4, pp. 1-50.
<i>V</i>	"Virtex-II 1.5V Field-Programmable Gate Arrays", Advance Product Specification, DS031-1 (v1.5), Xilinx Inc., April 2, 2001, Module 1 of 4, pp. 1-7.
	"Virtex-II 1.5V Field-Programmable Gate Arrays", Advance Product Specification, DS031-2 (v1.5), Xilinx Inc., April 2, 2001, Module 2 of 4, pp. 1-36.

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